IN THE CLAIMS

1 – 10 (canceled)

11. (currently amended) A flash memory system comprising:

a processor to process data;

a memory array storing a BIOS program to instruct the processor to generate an access code; and

a check register to store the access code generated by the processor, wherein the check register generates a write enable signal to the memory array in response to writes of the access code, the writing of the access code to the check register controlled by the BIOS program in response to a request from a flash utility program that is coupled to the processor.

12. (original) The flash memory system of claim 11 wherein the BIOS program instructs the processor to generate the access code at each system power up.

13 – 14 (canceled)

15. (currently amended) ~~The flash memory system of claim 13~~ A flash memory system comprising:

a processor to process data;

a memory array storing a BIOS program to instruct the processor to generate an access code; and

a check register to store the access code generated by the processor, wherein the check register generates a write enable signal to the memory array in response to writes of the access code, the writing of the access code to the check register controlled by the BIOS program wherein an external program requests the BIOS to write the access code to the check register.

16 – 22 (canceled)

23. (currently amended) A flash memory system comprising:

a memory array having a BIOS program;

a processor to execute the BIOS program;

control circuitry to control write operations to the memory array in response to a write enable signal; and

a check register to store a random access code generated by the BIOS program, wherein the check register gates the write enable signal to the control circuitry in response to the random access code and the check register is not located inside the flash memory that contains the flash memory array.

24. (original) The flash memory device of claim 23 wherein the random access code is stored in volatile memory so the random access code is erased when power is removed from the check register.

25. (original) The flash memory system of claim 23 wherein the memory array and the check register are embedded in a single flash memory.

26. (canceled)

27. (currently amended) ~~The flash memory system of claim 26 further comprising:~~
A flash memory system comprising:

a memory array having a BIOS program;

a processor to execute the BIOS program;

control circuitry to control write operations to the memory array in response to a write enable signal;

a check register to store a random access code generated by the BIOS program, wherein the check register gates the write enable signal to the control circuitry in response to the random access code and the check register is not located inside the flash memory that contains the flash memory array; and

a serial bus to couple the check register to the processor.

28. (canceled)

29. (currently amended) The flash memory system of claim 30 ~~28~~ wherein the random access code is specific to each boot cycle.

30. (currently amended) ~~The flash memory system of 28 wherein the program logic device further comprises:~~

A flash memory system comprising:

a memory array having a BIOS program stored therein;

control circuitry to control write operations to the memory array;

a processor to execute the BIOS program;

a program logic device to store a random access code generated by the processor from instructions contained in the BIOS program, wherein the program logic device gates a write enable signal to the control circuitry in response to the random access code;

a check register to send an active LOW write enable signal to the control circuitry in response to the random access code being written to the check register, wherein the control circuitry allows write operations to the memory array; and

a logic circuit to selectively send an inactive HIGH signal to the control circuitry after completion of the write operation to the flash memory array to disable write operations to the memory array.

31. (original) The flash memory system of 30 wherein an output of the processor supplying write enable signals is coupled to a first input of the logic circuit and an output of the check register is coupled to a second input of the logic circuit, further wherein an output of the logic circuit is coupled to the control circuitry.

32. (original) The flash memory system of claim 30 wherein the logic circuit performs an AND function.

33. (currently amended) The flash memory system of <u>30</u> ~~28~~ wherein the program logic device further comprises:

a check register to send an active HIGH write enable signal to the control circuitry in response to the random access code being written to the check register, wherein the control circuitry allows write operations to the memory array; and

a logic circuit to selectively send an inactive LOW signal to the control circuitry after completion of the write operation to the flash memory array to disable write operations to the memory array.

34. (original) The flash memory system of 33 wherein an output of the processor supplying write enable signals is coupled to a first input of the logic circuit and an output of the check register is coupled to a second input of the logic circuit, further wherein an output of the logic circuit is coupled to the control circuitry.

35. (original) The flash memory system of claim 33 wherein the logic circuit performs an AND function.

36 – 44 (canceled)

45. (original) A method of operating a flash memory system comprising:

powering up a flash memory;

executing a BIOS program;

generating a random access code in response to the executed BIOS program;

storing the random access code in a check register; and

toggling write enable signals of the flash memory in response to writes of the random access code to the check register.

46. (original) The method of claim 45 further comprising:

monitoring a write request to the flash memory for an authorization code; and

writing the access code to the check register if the write request has the authorization code.

47. (original) The method of claim 46 wherein a BIOS program controls writes of the random access code to the check register.

48. (original) The method of claim 46 wherein the BIOS program authenticates the authorization code.

49. (previously presented) A method of operating a flash memory system comprising:

generating a random access code at power up;

storing the random access code in a check register that controls a write enable signal to a flash memory;

executing a flash utility program containing instructions to write to the flash memory;

verifying the authenticity of the utility program;

toggling the check register to assert the write enable signal;

writing to the flash memory array; and

toggling the check register to disable the write enable signal.

50. (original) The method of claim 49 further comprising:

deleting the random access code when power is removed from the flash memory system.

51. (original) The method of claim 49 wherein a BIOS controls the toggling of the write enable

signals by writing the random access code to the check register.

52. (original) The method of claim 49 wherein the BIOS authenticates the flash utility program.

53. (previously presented) A method of operating a flash memory system comprising:

executing a flash utility program containing instructions to write to a flash memory array;

verifying the authenticity of the flash utility program with a BIOS program;

asserting a write enable signal if the flash utility program is authenticated; and

writing to the flash memory array.

54. (original) The method of claim 53 wherein the BIOS program controls the write enable signals.

55. (original) The method of claim 53 wherein the BIOS program writes an access code to a check register to toggle the write enable signals.

56 – 59 (canceled)